SPICE Models for Alpha AXP Microprocessors and Peripheral Chips: An Application Note

This application note provides information for design engineers who conduct Level 3 SPICE simulations of Alpha AXP microprocessors and peripheral chips. This document contains pin-to-model reference tables for the following components:

- DECchip 21030 PCI Graphics Accelerator
- DECchip 21040 Ethernet LAN Controller for PCI
- DECchip 21050 PCI-to-PCI Bridge
- DECchip 21064 Alpha AXP Microprocessor
- DECchip 21064A Alpha AXP Microprocessor
- DECchip 21066 and DECchip 21068 Alpha AXP Microprocessors
- DECchip 21071 and DECchip 21072 Core Logic Chipsets

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Contents

Preface

This preface provides information about the purpose, audience, and structure of the document: *SPICE Models for Alpha AXP Microprocessors and Peripheral Chips: An Application Note*. It also describes the conventions used in this document.

Document Purpose

This document contains pin-to-model reference tables that will assist in cross-referencing Level 3 SPICE models with Alpha AXP microprocessors and peripheral chips.

The following pin-to-model reference tables of Alpha AXP Microprocessor chips are included in Chapter 1:

- DECchip 21064 Alpha AXP Microprocessor
- DECchip 21064A Alpha AXP Microprocessor
- DECchip 21066 and DECchip 21068 Alpha AXP Microprocessors

The following pin-to-model reference tables of peripheral chips are included in Chapter 2:

- DECchip 21030 PCI Graphics Accelerator
- DECchip 21040 Ethernet LAN Controller for PCI
- DECchip 21050 PCI-to-PCI Bridge
- DECchip 21071 and DECchip 21072 Core Logic Chipsets

Intended Audience and Prerequisites

This application note is for users who are familiar with SPICE. This document provides information for system designers who will conduct simulations of SPICE models for the aforementioned Digital products.

SPICE Model Description

You can use the SPICE models to simulate either *Worst Case* (WC) or *Best Case* (BC) operating conditions. The SPICE model files contain subcircuits, which provide a description of the connectivity and the parameters to be used with the model.

Most of the input pins have only one subcircuit that functions for either operating condition. However, all of the driver pins and some of the input pins have two separate driver subcircuits that correspond to the two operating conditions. Either subcircuit may be instantiated for Level 3 SPICE simulation, depending on the operating condition desired.

Note

See the 0README.TXT file in the evaluation board kit for more information about the file and directory structure of the SPICE models.

Reference Table Conventions

All of the pin-to-model reference tables use the following conventions:

Convention	Description
Pin Name	The name of the signal pin on the chip.
Pin Type	Whether the pin is an input (I), output (O), or bidirectional (I/O) pin.
File Name of Model	The name of the SPICE model file for the pin.
Subcircuit Names ending with WC	Worst Case operating condition.
Subcircuit Names ending with BC	Best Case operating condition.
Extents	Specified by a pair of numbers in angle brackets (<>) separated by a colon (:) and are inclusive. For example, bits <0:3> indicates an extent including bits 0, 1, 2, and 3.

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Reference Tables for SPICE Models of Alpha AXP Microprocessors

1.1 DECchip 21064 Alpha AXP Microprocessor Pin-To-Model Reference Table

Table 1–1 lists all the pins and corresponding Level 3 SPICE model to use for the DECchip 21064 Alpha AXP Microprocessor. The subcircuits are simulated with the following *Worst Case* (WC) and *Best Case* (BC) operating conditions.

- Subcircuit names ending with WC have an operating condition of V_{dd} at 3.00 volts with a temperature of 85°C.
- Subcircuit names ending with BC have an operating condition of V_{dd} at 3.60 volts with a temperature of 25°C.

Table 1–1 DECchip 21064 Pins with Corresponding Models

Pin Name	Pin Type	File Name of Model	Model Subcircuits
adr_h<33:5>	I/O	B_21064.SPI	EDRVB-WC, EDRVB-BC
cAck_h<2:0>	I	I_21064.SPI	EIN
check_h<27:0>	I/O	B_21064.SPI	EDRVB-WC, EDRVB-BC
clkIn_h	I	C_21064.SPI	ECLK
clkIn_l	I	C_21064.SPI	ECLK
cont_l	I	I_21064.SPI	EIN
cpuClkOut_h	O	O_21064.SPI	EDRVO-WC, EDRVO-BC
cReq_h<2:0>	O	O_21064.SPI	EDRVO-WC, EDRVO-BC
cWMask_h<7:0>	O	O_21064.SPI	EDRVO-WC, EDRVO-BC
dataA_h<4:3>	O	O_21064.SPI	EDRVO-WC, EDRVO-BC
dataCEOE_h<3:0>	O	O_21064.SPI	EDRVO-WC, EDRVO-BC
dataWE_h<3:0>	O	O_21064.SPI	EDRVO-WC, EDRVO-BC
datA_h<127:0>	I/O	B_21064.SPI	EDRVB-WC, EDRVB-BC
dcOk_h	I	I_21064.SPI	EIN
dinvReq_h	I	I_21064.SPI	EIN
dMapWE_h	O	O_21064.SPI	EDRVO-WC, EDRVO-BC
dOE_l	I	I_21064.SPI	EIN
dRAck_h<2:0>	I	I_21064.SPI	EIN
dWSel_h<1:0>	I	I_21064.SPI	EIN

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Table 1–1 (Cont.) DECchip 21064 Pins with Corresponding Models

Pin Name	Pin Type	File Name of Model	Model Subcircuits
eclOut_h	I	Model not provided†	Subcircuit not provided
holdReq_h	I	I_21064.SPI	EIN
holdAck_h	O	O_21064.SPI	EDRVO-WC, EDRVO-BC
iAdr_h<12:5>	I	I_21064.SPI	EIN
icMode_h<1:0>	I	I_21064.SPI	EIN
irq_h<5:0>	I	I_21064.SPI	EIN
perf_cnt_h<1:0>	I	I_21064.SPI	EIN
reset_l	I	I_21064.SPI	EIN
sRomClk_h	O	O_21064.SPI	EDRVO-WC, EDRVO-BC
sRomD_h	I	I_21064.SPI	EIN
sRomOE_l	O	O_21064.SPI	EDRVO-WC, EDRVO-BC
sysClkOut1_h	O	O_21064.SPI	EDRVO-WC, EDRVO-BC
sysClkOut1_l	O	O_21064.SPI	EDRVO-WC, EDRVO-BC
sysClkOut2_h	O	O_21064.SPI	EDRVO-WC, EDRVO-BC
sysClkOut2_l	O	O_21064.SPI	EDRVO-WC, EDRVO-BC
tagadrP_h	I	I_21064.SPI	EIN
tagadr_h<33:17>	I	I_21064.SPI	EIN
tagCEOE_h	O	O_21064.SPI	EDRVO-WC, EDRVO-BC
tagCtlD_h	I/O	B_21064.SPI	EDRVB-WC, EDRVB-BC
tagCtlP_h	I/O	B_21064.SPI	EDRVB-WC, EDRVB-BC
tagCtlS_h	I/O	B_21064.SPI	EDRVB-WC, EDRVB-BC
tagCtlV_h	I/O	B_21064.SPI	EDRVB-WC, EDRVB-BC
tagCtlWE_h	O	O_21064.SPI	EDRVO-WC, EDRVO-BC
tagEq_l	O	O_21064.SPI	EDRVO-WC, EDRVO-BC
tagOk_l	I	I_21064.SPI	EIN
tagOk_h	I	I_21064.SPI	EIN
testClkIn_h	I	I_21064.SPI	EIN
testClkIn_l	I	I_21064.SPI	EIN
triState_l	I	I_21064.SPI	EIN
vRef	I	Model not provided‡	Subcircuit not provided

† eclOut_h is an unused pin and should be connected to V_{SS}.

‡ vRef should be connected to 1.4 volts.

1.2 DECchip 21064A Alpha AXP Microprocessor Pin-To-Model Reference Table

Table 1–2 lists all the pins and corresponding Level 3 SPICE model to use for the DECchip 21064A Alpha AXP Microprocessor. The subcircuits are simulated with the following *Worst Case* (WC) and *Best Case* (BC) operating conditions.

- Subcircuit names ending with WC have an operating condition of V_{dd} at 3.00 volts with a temperature of 85°C.
- Subcircuit names ending with BC have an operating condition of V_{dd} at 3.60 volts with a temperature of 25°C.

Table 1–2 DECchip 21064A Pins with Corresponding Models

Pin Name	Pin Type	File Name of Model	Model Subcircuits
adr_h<33:5>	I/O	B_21064A.SPI	FDRVB-WC, FDRVB-BC
cAck_h<2:0>	I	I_21064A.SPI	FIN
check_h<27:0>	I/O	B_21064A.SPI	FDRVB-WC, FDRVB-BC
clkIn_h	I	C_21064A.SPI	FCLK
clkIn_l	I	C_21064A.SPI	FCLK
cont_l	I	I_21064A.SPI	FIN
cpuClkOut_h	O	O_21064A.SPI	FDRVO-WC, FDRVO-BC
cReq_h<2:0>	O	O_21064A.SPI	FDRVO-WC, FDRVO-BC
cWMask_h<7:0>	O	O_21064A.SPI	FDRVO-WC, FDRVO-BC
dataA_h<4:3>	O	O_21064A.SPI	FDRVO-WC, FDRVO-BC
dataCEOE_h<3:0>	O	O_21064A.SPI	FDRVO-WC, FDRVO-BC
dataWE_h<3:0>	O	O_21064A.SPI	FDRVO-WC, FDRVO-BC
data_h<127:0>	I/O	B_21064A.SPI	FDRVB-WC, FDRVB-BC
dcOk_h	I	I_21064A.SPI	FIN
dInvReq_h<1:0>	I	I_21064A.SPI	FIN
dMapWE_h<1:0>	O	O_21064A.SPI	FDRVO-WC, FDRVO-BC
dOE_l	I	I_21064A.SPI	FIN
dRAck_h<2:0>	I	I_21064A.SPI	FIN
dWSel_h<1:0>	I	I_21064A.SPI	FIN
eclOut_h	I	Model not provided†	Subcircuit not provided
holdReq_h	I	I_21064A.SPI	FIN
holdAck_h	O	O_21064A.SPI	FDRVO-WC, FDRVO-BC
iAdr_h<12:5>	I	I_21064A.SPI	FIN
icMode_h<2:0>	I	I_21064A.SPI	FIN
irq_h<5:0>	I	I_21064A.SPI	FIN
perf_cnt_h<1:0>	I	I_21064A.SPI	FIN
reset_l	I	I_21064A.SPI	FIN
sRomClk_h	O	O_21064A.SPI	FDRVO-WC, FDRVO-BC

† eclOut_h is an unused pin and should be connected to V_{SS}.

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Table 1–2 (Cont.) DECchip 21064A Pins with Corresponding Models

Pin Name	Pin Type	File Name of Model	Model Subcircuits
sRomD_h	I	I_21064A.SPI	FIN
sRomOE_l	O	O_21064A.SPI	FDRVO-WC, FDRVO-BC
sysClkOut1_h	O	O_21064A.SPI	FDRVO-WC, FDRVO-BC
sysClkOut1_l	O	O_21064A.SPI	FDRVO-WC, FDRVO-BC
sysClkOut2_h	O	O_21064A.SPI	FDRVO-WC, FDRVO-BC
sysClkOut2_l	O	O_21064A.SPI	FDRVO-WC, FDRVO-BC
tagadrP_h	I	I_21064A.SPI	FIN
tagadr_h<33:18>	I	I_21064A.SPI	FIN
tagCEOE_h	O	O_21064A.SPI	FDRVO-WC, FDRVO-BC
tagCtlD_h	I/O	B_21064A.SPI	FDRVB-WC, FDRVB-BC
tagCtlP_h	I/O	B_21064A.SPI	FDRVB-WC, FDRVB-BC
tagCtlS_h	I/O	B_21064A.SPI	FDRVB-WC, FDRVB-BC
tagCtlV_h	I/O	B_21064A.SPI	FDRVB-WC, FDRVB-BC
tagCtlWE_h	O	O_21064A.SPI	FDRVO-WC, FDRVO-BC
tagOk_l	I	I_21064A.SPI	FIN
tagOk_h	I	I_21064A.SPI	FIN
testClkin_h	I	I_21064A.SPI	FIN
testClkin_l	I	I_21064A.SPI	FIN
triState_l	I	I_21064A.SPI	FIN
holdReq_h	I	I_21064A.SPI	FIN
irq_h<5:0>	I	I_21064A.SPI	FIN
resetSClk_h	I	I_21064A.SPI	FIN
lockFlag_h	O	O_21064A.SPI	FDRVO-WC, FDRVO-BC
lockWE_h	O	O_21064A.SPI	FDRVO-WC, FDRVO-BC
sysClkDiv_h	I	I_21064A.SPI	FIN
vRef	I	Model not provided‡	Subcircuits not provided

‡ vRef should be connected to 1.4 volts.

1.3 DECchip 21066 and DECchip 21068 Alpha AXP Microprocessor Pin-To-Model Reference Table

Table 1–3 lists all the pins and corresponding Level 3 SPICE model to use for the DECchip 21066 and DECchip 21068 Alpha AXP Microprocessors. The subcircuits are simulated with the following *Worst Case* (WC) and *Best Case* (BC) operating conditions.

- Subcircuit names ending with WC have an operating condition of V_{dd} at 3.00 volts with a temperature of 85°C.
- Subcircuit names ending with BC have an operating condition of V_{dd} at 3.60 volts with a temperature of 25°C.

Table 1–3 DECchip 21066 and 21068 Pins with Corresponding Models

Pin Name	Pin Type	File Name of Model	Model Subcircuits
	Memory Controller Pins (119 Total)		
mem_data<63:0>	I/O	T5_21066.SPI	LDRT5-WC, LDRT5-BC
mem_ecc<7:0>	I/O	T3_21066.SPI	LDRT3-WC, LDRT3-BC
mem_addr<11:0>	O	B3_21066.SPI	LDRB3-WC, LDRB3-BC
mem_write_l	O	U2_21066.SPI	LDRU2-WC, LDRU2-BC
mem_rasa_l<3:0>	O	U4_21066.SPI	LDRU4-WC, LDRU4-BC
mem_rasb_l<3:0>	O	U4_21066.SPI	LDRU4-WC, LDRU4-BC
mem_cas_l	O	U2_21066.SPI	LDRU2-WC, LDRU2-BC
mem_dtoe_l	O	U4_21066.SPI	LDRU4-WC, LDRU4-BC
mem_dsf	O	U4_21066.SPI	LDRU4-WC, LDRU4-BC
mem_rd_oe	O	D2_21066.SPI	LDRD2-WC, LDRD2-BC
mem_wr_oe_l	O	U2_21066.SPI	LDRU2-WC, LDRU2-BC
bc_tag<7:0>	I/O	T3_21066.SPI	LDRT3-WC, LDRT3-BC
bc_parity	I/O	T3_21066.SPI	LDRT3-WC, LDRT3-BC
bc_index	O	B3_21066.SPI	LDRB3-WC, LDRB3-BC
bc_idx_tag<4:0>	I/O	T3_21066.SPI	LDRT3-WC, LDRT3-BC
bc_cs_l	O	U2_21066.SPI	LDRU2-WC, LDRU2-BC
bc_we_l	O	O2_21066.SPI	LDRO2-WC, LDRO2-BC
bc_oe_l	O	O2_21066.SPI	LDRO2-WC, LDRO2-BC
bc_dirty	I/O	T3_21066.SPI	LDRT3-WC, LDRT3-BC
vframe_l	I	I_21066.SPI	LIN
vrefresh_l	I	I_21066.SPI	LIN

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Table 1–3 (Cont.) DECchip 21066 and 21068 Pins with Corresponding Models

Pin Name	Pin Type	File Name of Model	Model Subcircuits
PCI Bus Signal Pins (50 Total)			
ad<31:0>	I/O	B1_21066.SPI	LDRB1-WC, LDRB1-BC
c_be_l<3:0>	I/O	B1_21066.SPI	LDRB1-WC, LDRB1-BC
frame_l	I/O	B1_21066.SPI	LDRB1-WC, LDRB1-BC
trdly	I/O	B1_21066.SPI	LDRB1-WC, LDRB1-BC
irdyl	I/O	B1_21066.SPI	LDRB1-WC, LDRB1-BC
stop_l	I/O	B1_21066.SPI	LDRB1-WC, LDRB1-BC
par	I/O	B1_21066.SPI	LDRB1-WC, LDRB1-BC
perr_l	I/O	B1_21066.SPI	LDRB1-WC, LDRB1-BC
devsel_l	I/O	B1_21066.SPI	LDRB1-WC, LDRB1-BC
req_l	O	B1_21066.SPI	LDRB1-WC, LDRB1-BC
gnt_l	I	I_21066.SPI	LIN
rst_l	O	B1_21066.SPI	LDRB1-WC, LDRB1-BC
lock_l	I	I_21066.SPI	LIN
pci_clk_in	I	I_21066.SPI	LIN
memreq_l	I	I_21066.SPI	LIN
memack_l	O	O4_21066.SPI	LDRO4-WC, LDRO4-BC
Clock Pins (8 Total)			
pll_clk_in	I	Model not provided	Subcircuit not provided
pll_clk_in_l	I	Model not provided	Subcircuit not provided
pll_bypass	I	Model not provided	Subcircuit not provided
pll_i_ref	I	Model not provided	Subcircuit not provided
pll_filter	I	Model not provided	Subcircuit not provided
pll_5v	I	Model not provided	Subcircuit not provided
test_clk_out	O	O5_21066.SPI	LDRO5-WC, LDRO5-BC
reset_in_l	I	I_21066.SPI	LIN
JTAG Pins (5 Total)			
tdi	I	IU_21066.SPI	LINU-WC, LINU-BC
tdo	O	O5_21066.SPI	LDRO5-WC, LDRO5-BC
tms	I	IU_21066.SPI	LINU-WC, LINU-BC
tck	I	ID_21066.SPI	LIND-WC, LIND-BC
trst_l	I	IU_21066.SPI	LINU-WC, LINU-BC

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Table 1–3 (Cont.) DECchip 21066 and 21068 Pins with Corresponding Models

Pin Name	Pin Type	File Name of Model	Model Subcircuits
Interrupt, Serial ROM Interface, and instr_ref Pins (7 Total)			
irq<2:0>	I	I_21066.SPI	LIN
sromoe_l	O	O5_21066.SPI	LDRO5-WC, LDRO5-BC
sromd	I	I_21066.SPI	LIN
sromclk	O	O5_21066.SPI	LDRO5-WC, LDRO5-BC
instr_ref	O	O2_21066.SPI	LDRO2-WC, LDRO2-BC

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Reference Tables for SPICE Models of Peripheral Chips

2.1 DECchip 21030 PCI Graphics Accelerator Pin-To-Model Reference Table

Table 2–2 lists all the signal pins and corresponding Level 3 SPICE model to use for the DECchip 21030 PCI Graphics Accelerator. The subcircuits are simulated with the following *Worst Case* (WC) and *Best Case* (BC) operating conditions.

- Subcircuit names ending with WC have an operating condition of V_{dd} at 4.75 volts with a temperature of 85°C.
- Subcircuit names ending with BC have an operating condition of V_{dd} at 5.25 volts with a temperature of 25°C.

Each driver pin has one of four different subcircuits associated with it, as shown in Table 2–1.

Table 2–1 Characteristics of Driver Subcircuits for the 21030 Chip

Subcircuits	Characteristics
GDRVA-WC, GDRVA-BC	12/16 mA†
GDRVB-WC, GDRVB-BC	4 mA with slew rate control
GDRVC-WC, GDRVC-BC	4 mA, open drain output with slew rate control
GDRVO-WC, GDRVO-BC	4 mA, output only with slew rate control

†The value of 12 mA or 16 mA depends on whether the driver is sourcing or sinking current.

Table 2–2 DECchip 21030 Pins with Corresponding Models

Pin Name	Pin Type	File Name of Model	Model Subcircuits
Frame Buffer Interface Pins (123 Total)			
addr<17:0>	O	O_21030.SPI	GDRVO-WC, GDRVO-BC
addren_l<1:0>	O	O_21030.SPI	GDRVO-WC, GDRVO-BC
cas_l<3:0>	O	O_21030.SPI	GDRVO-WC, GDRVO-BC
casen<1:0>	O	O_21030.SPI	GDRVO-WC, GDRVO-BC
casmode<1:0>	O	O_21030.SPI	GDRVO-WC, GDRVO-BC
dsf<1:0>	O	O_21030.SPI	GDRVO-WC, GDRVO-BC
oe_l<1:0>	O	O_21030.SPI	GDRVO-WC, GDRVO-BC
ras_l<3:0>	O	O_21030.SPI	GDRVO-WC, GDRVO-BC
rasen_l<3:0>	O	O_21030.SPI	GDRVO-WC, GDRVO-BC
we_l<7:0>	O	O_21030.SPI	GDRVO-WC, GDRVO-BC
dacc<2:0>	O	O_21030.SPI	GDRVO-WC, GDRVO-BC
dacce_l<1:0>	O	O_21030.SPI	GDRVO-WC, GDRVO-BC
dacrw	O	O_21030.SPI	GDRVO-WC, GDRVO-BC
data<63:0>	I/O	B4_21030.SPI	GDRVB-WC, GDRVB-BC
fbclk	I	I_21030.SPI	GIN
isce_l	O	O_21030.SPI	GDRVO-WC, GDRVO-BC
romce_l	O	O_21030.SPI	GDRVO-WC, GDRVO-BC
romoe_l	O	O_21030.SPI	GDRVO-WC, GDRVO-BC
romwe_l	O	O_21030.SPI	GDRVO-WC, GDRVO-BC
PCI Interface Pins (48 Total)			
ad<31:0>	I/O	B6_21030.SPI	GDRVA-WC, GDRVA-BC
cbe_l<3:0>	I/O	B6_21030.SPI	GDRVA-WC, GDRVA-BC
devsel_l	I/O	B6_21030.SPI	GDRVA-WC, GDRVA-BC
frame_l	I/O	B6_21030.SPI	GDRVA-WC, GDRVA-BC
gnt_l	I	I_21030.SPI	GIN
idsel	I	I_21030.SPI	GIN
inta_l	O	C_21030.SPI	GDRVC-WC, GDRVC-BC
irdy_l	I/O	B6_21030.SPI	GDRVA-WC, GDRVA-BC
par	I/O	B6_21030.SPI	GDRVA-WC, GDRVA-BC
pciclk	I	I_21030.SPI	GIN
req_l	O	B6_21030.SPI†	GDRVA-WC, GDRVA-BC
rst	I	I_21030.SPI	GIN
stop_l	I/O	B6_21030.SPI	GDRVA-WC, GDRVA-BC
trdy_l	I/O	B6_21030.SPI	GDRVA-WC, GDRVA-BC

†The req_l pin, which is an output, does not use the input stage of this bidirectional subcircuit.

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Table 2–2 (Cont.) DECchip 21030 Pins with Corresponding Models

Pin Name	Pin Type	File Name of Model	Model Subcircuits
		Video Interface Pins (14 Total)	
blank_l	O	O_21030.SPI	GDRVO-WC, GDRVO-BC
cursor<7:0>	O	O_21030.SPI	GDRVO-WC, GDRVO-BC
hold_l	O	O_21030.SPI	GDRVO-WC, GDRVO-BC
hsync_l	O	O_21030.SPI	GDRVO-WC, GDRVO-BC
toggle	O	O_21030.SPI	GDRVO-WC, GDRVO-BC
vidclk	I	I_21030.SPI	GIN
vsync_l	O	O_21030.SPI	GDRVO-WC, GDRVO-BC

2.2 DECchip 21040 Ethernet LAN Controller for PCI Pin-To-Model Reference Table

Table 2–3 lists all the PCI bus interface pins and corresponding Level 3 SPICE model to use for the DECchip 21040 Ethernet LAN Controller for PCI. The subcircuits are simulated with the following *Worst Case* (WC) and *Best Case* (BC) operating conditions.

- Subcircuit names ending with WC have an operating condition of V_{dd} at 3.00 volts with a temperature of 85°C.
- Subcircuit names ending with BC have an operating condition of V_{dd} at 3.60 volts with a temperature of 25°C.

Table 2–3 DECchip 21040 Pins with Corresponding Models

Pin Name	Pin Type	File Name of Model	Model Subcircuits
AD<31:0>	I/O	B_21040.SPI	TDRVB-WC, TDRVB-BC
C/BE_L<3:0>	I/O	B_21040.SPI	TDRVB-WC, TDRVB-BC
FRAME_L	I/O	B_21040.SPI	TDRVB-WC, TDRVB-BC
TRDY_L	I/O	B_21040.SPI	TDRVB-WC, TDRVB-BC
IRDY_L	I/O	B_21040.SPI	TDRVB-WC, TDRVB-BC
STOP_L	I/O	B_21040.SPI	TDRVB-WC, TDRVB-BC
REQ_L	O	O_21040.SPI	TDRVO-WC, TDRVO-BC
GNT_L	I	I_21040.SPI	TIN
IDSEL	I	I_21040.SPI	TIN
DEVSEL_L	I/O	B_21040.SPI	TDRVB-WC, TDRVB-BC
PAR	I/O	B_21040.SPI	TDRVB-WC, TDRVB-BC
INT_L	O	O_21040.SPI	TDRVO-WC, TDRVO-BC
CLK	I	I_21040.SPI	TIN
RST	I	I_21040.SPI	TIN

2.3 DECchip 21050 PCI-to-PCI Bridge Pin-To-Model Reference Table

Table 2–4 lists all the signal pins and corresponding Level 3 SPICE model to use for the DECchip 21050 PCI-to-PCI Bridge. The subcircuits are simulated with the following *Worst Case* (WC) and *Best Case* (BC) operating conditions.

- Subcircuit names ending with WC have an operating condition of V_{dd} at 4.75 volts with a temperature of 85°C.
- Subcircuit names ending with BC have an operating condition of V_{dd} at 5.25 volts with a temperature of 25°C.

Table 2–4 DECchip 21050 Pins with Corresponding Models

Pin Name	Pin Type	File Name of Model	Model Subcircuits
go_z	I	I_21050.SPI	BIN
nand_out	O	O_21050.SPI	BDRVO-WC, BDRVO-BC
p_ad<31:0>	I/O	B_21050.SPI	BDRVB-WC, BDRVB-BC
p_cbe_l<3:0>	I/O	B_21050.SPI	BDRVB-WC, BDRVB-BC
p_clk	I	I_21050.SPI	BIN
p_devsel_l	I/O	B_21050.SPI	BDRVB-WC, BDRVB-BC
p_frame_l	I/O	B_21050.SPI	BDRVB-WC, BDRVB-BC
p_gnt_l	I	I_21050.SPI	BIN
p_idsel	I	I_21050.SPI	BIN
p_irdy_l	I/O	B_21050.SPI	BDRVB-WC, BDRVB-BC
p_lock_l	I/O	B_21050.SPI	BDRVB-WC, BDRVB-BC
p_par	I/O	B_21050.SPI	BDRVB-WC, BDRVB-BC
p_perr_l	I/O	B_21050.SPI	BDRVB-WC, BDRVB-BC
p_req_l	O	O_21050.SPI	BDRVO-WC, BDRVO-BC
p_rst_l	I	I_21050.SPI	BIN
p_serr_l	I/O	Model not provided	Subcircuit not provided
p_stop_l	I/O	B_21050.SPI	BDRVB-WC, BDRVB-BC
p_trdy_l	I/O	B_21050.SPI	BDRVB-WC, BDRVB-BC
s_ad<31:0>	I/O	B_21050.SPI	BDRVB-WC, BDRVB-BC
s_bufne_l	O	O_21050.SPI	BDRVO-WC, BDRVO-BC
s_cbe_l<3:0>	I/O	B_21050.SPI	BDRVB-WC, BDRVB-BC
s_cfn_l	I	I_21050.SPI	BIN
s_clk	I	I_21050.SPI	BIN
s_clk_o<6:0>	O	C_21050.SPI	BDRVC-WC, BDRVC-BC
s_devsel_l	I/O	B_21050.SPI	BDRVB-WC, BDRVB-BC
s_dispst_l	I	I_21050.SPI	BIN
s_frame_l	I/O	B_21050.SPI	BDRVB-WC, BDRVB-BC

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Table 2–4 (Cont.) DECchip 21050 Pins with Corresponding Models

Pin Name	Pin Type	File Name of Model	Model Subcircuits
s_gnt_l<5:0>	O	O_21050.SPI	BDRVO-WC, BDRVO-BC
s_irdy_l	I/O	B_21050.SPI	BDRVB-WC, BDRVB-BC
s_lock_l	I/O	B_21050.SPI	BDRVB-WC, BDRVB-BC
s_par	I/O	B_21050.SPI	BDRVB-WC, BDRVB-BC
s_perr_l	I/O	B_21050.SPI	BDRVB-WC, BDRVB-BC
s_req_l<5:0>	I	I_21050.SPI	BIN
s_rst_l	O	O_21050.SPI	BDRVO-WC, BDRVO-BC
s_serr_l	I	I_21050.SPI	BIN
s_stop_l	I/O	B_21050.SPI	BDRVB-WC, BDRVB-BC
s_trdy_l	I/O	B_21050.SPI	BDRVB-WC, BDRVB-BC

2.4 DECchip 21071 and 21072 Core Logic Chipsets Pin-To-Model Reference Tables

The DECchip 21071 and DECchip 21072 core logic chipsets contain three types of chips: DECchip 21071–BA, DECchip 21071–CA, and DECchip 21071–DA. The DECchip 21071 chipset contains two data path chips and supports a 64-bit memory configuration; the DECchip 21072 contains four data path chips and supports a 128-bit memory configuration.

Table 2–5 lists the contents of the DECchip 21071 and DECchip 21072 core logic chipsets.

Table 2–5 Contents of 21071 and 21072 Chipsets

Chips	Function	Number of Chips for the 21071	Number of Chips for the 21072
DECchip 21071–BA	Data path	2	4
DECchip 21071–CA	Cache and memory controller	1	1
DECchip 21071–DA	PCI interface	1	1

The pins of the DECchip 21071 and 21072 chipsets, and which Level 3 SPICE model to use are described in Sections 2.4.1, 2.4.2, and 2.4.3. The subcircuits are simulated with the following *Worst Case* (WC) and *Best Case* (BC) operating conditions.

- Subcircuit names ending with WC have an operating condition of V_{dd} at 4.75 volts with a temperature of 85°C.
- Subcircuit names ending with BC have an operating condition of V_{dd} at 5.25 volts with a temperature of 25°C.

Each driver pin has one of three different subcircuits associated with it, as shown in Table 2–6.

Table 2–6 Characteristics of Driver Subcircuits for the 21071 and 21072 Chipsets

Subcircuits	Characteristics
ADRVA-WC, ADRVA-BC	12/16 mA†
ADRVB-WC, ADRVB-BC	8 mA
ADRVC-WC, ADRVC-BC	4 mA

†The value of 12 mA or 16 mA depends on whether the driver is sourcing or sinking current.

2.4.1 DECchip 21071–BA Pin-To-Model Reference Table

Table 2–7 lists all the pins and corresponding Level 3 SPICE model to use for the DECchip 21071–BA chip.

Table 2–7 DECchip 21071–BA Pins with Corresponding Models

Pin Name	Pin Type	File Name of Model	Model Subcircuits
CPU and Bcache Signal Pins (66 Total)			
sysData<31:0>	I/O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
sysPar<1:0>	I/O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
memData<31:0>	I/O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
memPar	I/O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
Cache and Memory Control Interface Signal Pins (13 Total)			
sysCMD<2:0>	I	I_21071.SPI	AIN
subCMD<1:0>	I	I_21071.SPI	AIN
sysIORead	I	I_21071.SPI	AIN
drvSysData	I	I_21071.SPI	AIN
drvsysCSR	I	I_21071.SPI	AIN
drvMemData	I	I_21071.SPI	AIN
memCMD<3:1>	I	I_21071.SPI	AIN
sysReadOW	I	I_21071.SPI	AIN
epiBus Signals (46 Total)			
epiData<31:0>	I/O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
epiBEnErr<3:0>	I/O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
epiOWSel	I	I_21071.SPI	AIN
epiLineSel<1:0>	I	I_21071.SPI	AIN
epiSelDMA	I	I_21071.SPI	AIN
epiFromIOB	I	I_21071.SPI	AIN
epiEnable<1:0>	I	I_21071.SPI	AIN
ioLineSel<1:0>	I	I_21071.SPI	AIN
epiLineInval	I	I_21071.SPI	AIN

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Table 2–7 (Cont.) DECchip 21071–BA Pins with Corresponding Models

Pin Name	Pin Type	File Name of Model	Model Subcircuits
Clock and Miscellaneous Signal Pins (8 Total)			
eccMode	I	I_21071.SPI	AIN
WideMem	I	I_21071.SPI	AIN
clk1x2	I	I_21071.SPI	AIN
clk2ref	I	I_21071.SPI	AIN
reset_l	I	I_21071.SPI	AIN
testMode	I	I_21071.SPI	AIN
tristate_l	I	I_21071.SPI	AIN
pTestout	O	B4_21071.SPI	ADRVC-WC, ADRVC-BC

2.4.2 DECchip 21071–CA Pin-To-Model Reference Table

Table 2–8 lists all the pins and corresponding Level 3 SPICE model to use for the DECchip 21071–CA chip.

Table 2–8 DECchip 21071–CA Pins with Corresponding Models

Pin Name	Pin Type	File Name of Model	Model Subcircuits
		CPU and Bcache Signals (85 Total)	
sysData<15:0>	I/O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
sysADR<33:5>	I	I_21071.SPI	AIN
tagAdr<31:17>	I/O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
tagAdrP	I/O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
tagCtlV	I/O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
tagCtlD	I/O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
tagCtlP	I/O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
cpuCReq<2:0>	I	I_21071.SPI	AIN
cpuCAck<2:0>	I/O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
cpuDRAck<2:0>	I/O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
cpuCWMask<7:0>	I/O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
cpuDWSel<1>	O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
cpuDInvReq	O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
cpuHoldReq	O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
cpuHoldAck	I	I_21071.SPI	AIN
		Bcache PAL Signals (9 Total)	
sysDOE	O	B8_21071.SPI	ADRVB-WC, ADRVB-BC
sysEarlyOEEn	O	B8_21071.SPI	ADRVB-WC, ADRVB-BC
sysTagOEEn	O	B8_21071.SPI	ADRVB-WC, ADRVB-BC
sysDataOEEn	O	B8_21071.SPI	ADRVB-WC, ADRVB-BC
sysDataWEEn	O	B8_21071.SPI	ADRVB-WC, ADRVB-BC
sysDataLongWE	O	B8_21071.SPI	ADRVB-WC, ADRVB-BC
sysTagWE	O	B8_21071.SPI	ADRVB-WC, ADRVB-BC
sysDatAALEn	O	B8_21071.SPI	ADRVB-WC, ADRVB-BC
sysDataAHEn	O	B8_21071.SPI	ADRVB-WC, ADRVB-BC
		PCI Bridge Interface Signals (9 Total)	
ioRequest<1:0>	I	I_21071.SPI	AIN
ioGrant	O	B8_21071.SPI	ADRVB-WC, ADRVB-BC
ioCmd<2:0>	I	I_21071.SPI	AIN
ioCAck<1:0>	O	B8_21071.SPI	ADRVB-WC, ADRVB-BC
ioDataRdy	O	B8_21071.SPI	ADRVB-WC, ADRVB-BC

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Table 2–8 (Cont.) DECchip 21071–CA Pins with Corresponding Models

Pin Name	Pin Type	File Name of Model	Model Subcircuits
Memory Signals (39 Total)			
memAdr<11:0>	O	B8_21071.SPI	ADRVB-WC, ADRVB-BC
memRAS_l<8:0>	O	B8_21071.SPI	ADRVB-WC, ADRVB-BC
memRASB_l<8:0>	O	B8_21071.SPI	ADRVB-WC, ADRVB-BC
memCAS_l<3:0>	O	B8_21071.SPI	ADRVB-WC, ADRVB-BC
memWE_l<1:0>	O	B8_21071.SPI	ADRVB-WC, ADRVB-BC
memPDClk	O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
memPDLoad_l	O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
memPDDIn	O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
Video Support Signals (4 Total)			
vFrame_l	I	I_21071.SPI	AIN
vRefresh_l	I	I_21071.SPI	AIN
memDTOE_l	O	B8_21071.SPI	ADRVB-WC, ADRVB-BC
memDSF	O	B8_21071.SPI	ADRVB-WC, ADRVB-BC
Data Path Signals (16 Total)			
sysCmd<2:0>	O	B8_21071.SPI	ADRVB-WC, ADRVB-BC
subCmdA<1:0>	O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
subCmdB<1:0>	O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
subCmdCommon	O	B8_21071.SPI	ADRVB-WC, ADRVB-BC
sysIORead	O	B8_21071.SPI	ADRVB-WC, ADRVB-BC
drvSysData	O	B8_21071.SPI	ADRVB-WC, ADRVB-BC
drvSysCSR	O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
drvMemData	O	B8_21071.SPI	ADRVB-WC, ADRVB-BC
memCMD<3:1>	O	B8_21071.SPI	ADRVB-WC, ADRVB-BC
sysReadOW	O	B8_21071.SPI	ADRVB-WC, ADRVB-BC
Miscellaneous and Clock Signals (8 Total)			
wideMem	I	I_21071.SPI	AIN
clk1x2	I	I_21071.SPI	AIN
clk2ref	I	I_21071.SPI	AIN
reset_l	I	I_21071.SPI	AIN
testMode	I	I_21071.SPI	AIN
scanEnable	I	I_21071.SPI	AIN
tristate_l	I	I_21071.SPI	AIN
pTestout	I	I_21071.SPI	AIN

2.4.3 DECchip 21071–DA Pin-To-Model Reference Table

Table 2–9 lists all the pins and corresponding Level 3 SPICE model to use for the DECchip 21071–DA chip.

Table 2–9 DECchip 21071–DA Pins with Corresponding Models

Pin Name	Pin Type	File Name of Model	Model Subcircuits
sysBus Signals (50 Total)			
sysAdr<33:5>	I/O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
cpuCReq<2:0>	I	I_21071.SPI	AIN
cpuCWMask<7:0>	I	I_21071.SPI	AIN
cpuHoldAck	I	I_21071.SPI	AIN
ioCmd<2:0>	I/O	B8_21071.SPI	ADRVB-WC, ADRVB-BC
ioCAck	I	I_21071.SPI	AIN
ioDataRdy	I	I_21071.SPI	AIN
ioLineSel<1:0>	O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
ioRequest<1:0>	O	B8_21071.SPI	ADRVB-WC, ADRVB-BC
ioGrant	I	I_21071.SPI	AIN
PCI Pins (47 Total)			
AD<31:0>	I/O	B6_21071.SPI	ADRVA-WC, ADRVA-BC
CBE_l<3:0>	I/O	B6_21071.SPI	ADRVA-WC, ADRVA-BC
Par	I/O	B6_21071.SPI	ADRVA-WC, ADRVA-BC
FrameL	I/O	B6_21071.SPI	ADRVA-WC, ADRVA-BC
TrdyL	I/O	B6_21071.SPI	ADRVA-WC, ADRVA-BC
IrdyL	I/O	B6_21071.SPI	ADRVA-WC, ADRVA-BC
StopL	I/O	B6_21071.SPI	ADRVA-WC, ADRVA-BC
PerrL	I/O	B6_21071.SPI	ADRVA-WC, ADRVA-BC
LockL	I/O	B6_21071.SPI	ADRVA-WC, ADRVA-BC
DevselL	I/O	B6_21071.SPI	ADRVA-WC, ADRVA-BC
ReqL	I/O	B6_21071.SPI	ADRVA-WC, ADRVA-BC
GntL	I/O	B6_21071.SPI	ADRVA-WC, ADRVA-BC
pClk	I	I_21071.SPI	AIN
PCI Sideband Pins (2 Total)			
MemReql	I	I_21071.SPI	AIN
MemAckl	O	B6_21071.SPI	ADRVA-WC, ADRVA-BC

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Table 2–9 (Cont.) DECchip 21071–DA Pins with Corresponding Models

Pin Name	Pin Type	File Name of Model	Model Subcircuits
epiBus Pins (46 Total)			
epiData<31:0>	I/O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
epiBEnErr<3:0>	I/O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
epiOWSel	O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
epiLineSel<1:0>	O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
epiSelDMA	O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
epiFromIOB	O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
epiEnable<3:0>	O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
epiLineInval	O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
Miscellaneous and Clock Signals (4 Total)			
intHw0	O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
resetL	I	I_21071.SPI	AIN
clk1x2	I	I_21071.SPI	AIN
clk2ref	I	I_21071.SPI	AIN
Test Signals (4 Total)			
PTestOut	O	B4_21071.SPI	ADRVC-WC, ADRVC-BC
Tristate_l	I	I_21071.SPI	AIN
testMode	I	I_21071.SPI	AIN
scanEn	I	I_21071.SPI	AIN

A

Technical Support, Ordering, and Associated Literature

This appendix describes how to obtain DECchip information and technical support, and order DECchip products and associated literature.

A.1 Calling the DECchip Information Line for Information and Technical Support

Call the DECchip Information Line for information and technical support:

United States and Canada	**1–800–332–2717**
TTY (United States only)	**1–800–332–2515**
Outside North America	**+1–508–568–6868**

A.2 Ordering DECchip Products

To order Alpha AXP microprocessors and related products, contact your local Digital sales office. Your sales representative may be able to help you take advantage of discounts and volume pricing.

To order DECchip samples or Sample Kits call **1–800–DIGITAL**.

You can order the following DECchip products from Digital:

Product	Speed	Order Number
Alpha AXP Microprocessors and Peripheral Chips		
DECchip 21030 PCI Graphics Accelerator	–	21030–AA
DECchip 21040 Ethernet LAN Controller for PCI	–	21040–AA
DECchip 21050 PCI-to-PCI Bridge	–	21050-AA
DECchip 21064–150 Alpha AXP Microprocessor	150 MHz	21064–AA
DECchip 21064–166 Alpha AXP Microprocessor	166 MHz	21064–CA
DECchip 21064–200 Alpha AXP Microprocessor	200 MHz	21064–BA
DECchip 21064A–233 Alpha AXP Microprocessor	233 MHz	21064–BB
DECchip 21064A–275 Alpha AXP Microprocessor	275 MHz	21064–DB
DECchip 21066–166 Alpha AXP Microprocessor	166 MHz	21066–AA
DECchip 21068–66 Alpha AXP Microprocessor	66 MHz	21068–AA
DECchip 21071 Core Logic Chipset	33 MHz	21071–AA
DECchip 21072 Core Logic Chipset	33 MHz	21072–AA

Product	Speed	Order Number
Evaluation Board Kits		
DECchip 21040 PCI Evaluation Board Kit	–	21A40–01
DECchip 21064–150 Evaluation Board OSF/1 and Windows NT	150 MHz	21A01–03
DECchip 21064–200 PCI Evaluation Board OSF/1 and Windows NT	200 MHz	21A02–01
DECchip 21064–275 PCI Evaluation Board OSF/1 and Windows NT	275 MHz	21A02–02
DECchip 21066 and DECchip 21068 Evaluation Board OSF/1 and Windows NT	166 MHz	21A03–02

A.3 Ordering Associated DECchip Literature

DECchip documentation and literature is available with the products. For a complete list and for information about ordering, contact the DECchip Information Line.