AlphaServer 8200/8400 System Technical Manual Supplement: CPU

Order Number: EK–T8030–TS. A01

The KN7CE CPU is based on a 440 MHz enhanced version of the Alpha 21164 microprocessor. Design changes on the KN7CE enable it to support MEMORY CHANNEL and deliver higher performance. The *AlphaServer 8200/ 8400 System Technical Manual* provides a full description of the CPU module. This document highlights the differences between the KN7CE and its two predecessors, and supplements information in the *AlphaServer 8200/ 8400 System Technical Manual*.

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Contents

Preface

Intended Audience

This document is intended for developers of system software and for service personnel working with AlphaServer 8200/8400 systems that use KN7CE CPU modules. It supplements the *AlphaServer 8200/ 8400 System Technical Manual* (EK–T8030–TM) that adequately covers the KN7CC and KN7CD CPU modules.

Document Structure

The material is presented in three chapters.

Chapter 1, **Introduction,** gives the areas of the KN7CE module where design changes have been made.

Chapter 2, **Register Functions,** describes changes made to the register file.

Chapter 3, **MEMORY CHANNEL Overview,** gives a synopsis of the MEMORY CHANNEL hardware.

Documentation Titles

Table 1 lists the manuals that document the MEMORY CHANNEL hardware.

Table 1 Memory Channel Hardware Documentation

Title	Order Number
MEMORY CHANNEL User's Guide	EK–PCIRM–UG
MEMORY CHANNEL Service Information	EK–PCIRM–SV

Chapter 1

Introduction

The KN7CE CPU module introduces enhanced features in three major areas:

- B-cache
- Register functions
- MEMORY CHANNEL

The KN7CE CPU features a 4-Mbyte baseline B-cache. ASICs designed into the module support both a 4-Mbyte B-cache and an 8-Mbyte B-cache. Modified registers are reproduced in full but the changes are emphasized. The KN7CE supports MEMORY CHANNEL, which is discussed in two documents listed in Table 1 in the Preface.

Chapter 2

Register Functions

2.1 Summary of Changes

Design changes have been made in the following registers for the KN7CE:

- **TLMODCONFIG register**
  Changes have been made to the register bit functions.
- **TLEPAERR register**
  Bit fields <23:20> and <14:13> have been redefined.
- **TLEP_VMG register**
  The function of this register is not implemented in the KN7CE modules. Thus, margining of 3.3V and 2.2/2.5V is not possible on the KN7CE.
- **TL56WERR registers**
  This register set is added to help in the diagnosis of the Ibox Timeout errors.
- **GBUS$MISCR register**
  The B-cache size field has been redefined to indicate an 8-Mbyte cache size.

2.2 Descriptions of Changes

Descriptions of functional modifications to the registers in the KN7CE module are given next.

TLMODCONFIG—CPU Module Configuration Register

Address BB + 10C0
Access R/W

The TLMODCONFIG register is set by console code to show the module configuration. The fields in this register determine much of the CPU module's setup and control such attributes as ADG queue depth thresholds and B-cache idle timing.

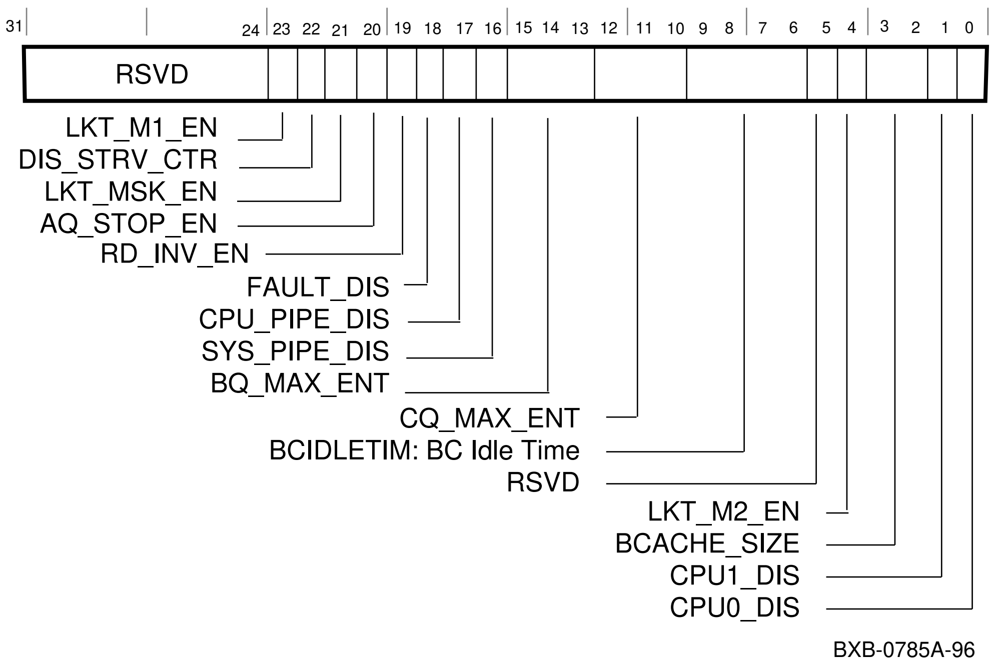

Table 2-1 TLMODCONFIG Register Bit Definitions

Name	Bit(s)	Type	Function
RSVD	<31:25>	R/W, 0	**Reserved.** Must be written as zeros.
RSVD	<24>	R/W, 0	**Reserved.** Must be written as zero. If set, an Undefined operation results.

Table 2-1 TLMODCONFIG Register Bit Definitions (Continued)

Name	Bit(s)	Type	Function
LKT_M1_EN	<23>	R/W, 0	**Lockout Mode 1 Enable.** The ADG implements two methods for responding to TLSB_LOCKOUT. This bit enables the original lockout logic, Lockout Mode 1. Mode 1 is the preferred method for responding to TLSB_LOCKOUT. Typically, therefore, Lockout Mode 2 is not used.
DIS_STRV_CTR	<22>	R/W, 1	**Disable Starvation Counter.** Sustained or repetitious system probe traffic can result in CPU chip starvation. Logic is provided in the ADG to detect starvation and allow CPU progress. This bit disables the starvation logic.
LKT_MSK_EN	<21>	R/W, 0	**Lockout Mask Enable.** When set, enables a counter circuit that periodically deasserts TLSB_LOCKOUT in the event that this signal is asserted for many cycles. This function is meant to be a debug feature only.
AQ_STOP_EN	<20>	R/W, 0	**Address Queue Stop Enable.** When set, enables a mode that prevents the ADG from overwriting entries in the address queue before the entries have been retired in the cache queues and the bus queue. Although a similar effect can be obtained by limiting the cache queue maximum entries to 2, this is the preferred method.
RD_INV_EN	<19>	R/W, 0	**Read Invalidate Enable.** When set, enables the read invalidate mode. When in this mode, the ADG invalidates cache blocks in response to Read_Miss_ Modify commands.
FAULT_DIS	<18>	R/W, 0	**Fault Disable.** When set, disables the CPU module from asserting TLSB_FAULT. This function is meant to be a debug feature only.
CPU_PIPE_DIS	<17>	R/W, 0	**CPU Pipe Disable.** When set, disables the piping of commands to the system from the CPUs. This function is meant to be a debug feature only.
SYS_PIPE_DIS	<16>	R/W, 0	**System Pipe Disable.** When set, disables the piping of commands to the CPUs from the system. This function is meant to be a debug feature only.
BQ_MAX_ENT	<15:13>	R/W, 4	**Bus Queue Maximum Entries.** Specifies the maximum number of bus queue entries supported. Smaller values than the default value of 4 can be programmed for this field for debug.

Table 2-1 TLMODCONFIG Register Bit Definitions (Continued)

<table>
<tr><th>Name</th><th>Bit(s)</th><th>Type</th><th>Function</th></tr>
<tr><td>CQ_MAX_ENT</td><td><12:10></td><td>R/W, 2</td><td>Cache Queue Maximum Entries. Specifies the maximum number of cache queue entries supported.</td></tr>
<tr><td>BCIDLETIM</td><td><9:6></td><td>R/W, F</td><td>B-Cache Idle Time. Specifies the assertion characteristics of the BC_Idle signal. Specifically, the encodings of this field indicate an assertion start time relative to a read command on the TLSB, and an assertion duration. The following table shows the BCDLETIM encodings. B0 refers to the cycle in which a read command is on the TLSB; B1 refers to the cycle after the read command is on the TLSB; B2 refers to the cycle that is two cycles after a read command is on the TLSB, and so on. The nominal value for the Duration for a 437 MHz 21164 chip is A (hex).
<table>
<tr><th><BCIDLETIM></th><th>Assert Time</th><th>Duration(cycles)</th></tr>
<tr><td>0</td><td>B0</td><td>7</td></tr>
<tr><td>1</td><td>B0</td><td>8</td></tr>
<tr><td>2</td><td>B0</td><td>9</td></tr>
<tr><td>3</td><td>B0</td><td>10</td></tr>
<tr><td>4</td><td>B2</td><td>7</td></tr>
<tr><td>5</td><td>B2</td><td>8</td></tr>
<tr><td>6</td><td>B2</td><td>9</td></tr>
<tr><td>7</td><td>B2</td><td>6</td></tr>
<tr><td>8</td><td>B1</td><td>7</td></tr>
<tr><td>9</td><td>B1</td><td>8</td></tr>
<tr><td>A</td><td>B1</td><td>9</td></tr>
<tr><td>B</td><td>B1</td><td>10</td></tr>
<tr><td>C</td><td>B1</td><td>7</td></tr>
<tr><td>D</td><td>B1</td><td>8</td></tr>
<tr><td>E</td><td>B1</td><td>9</td></tr>
<tr><td>F</td><td>B1</td><td>6</td></tr>
</table></td></tr>
<tr><td>RSVD</td><td><5></td><td>R/W, 0</td><td>Reserved. Must be written as zeros.</td></tr>
</table>

Table 2-1 TLMODCONFIG Register Bit Definitions (Continued)

<table>
<tr><th>Name</th><th>Bit(s)</th><th>Type</th><th>Function</th></tr>
<tr><td>LKT_M2_EN</td><td><4></td><td>R/W, 1</td><td>Lockout Mode 2 Enable. When set, enables the updated version of the lockout logic, which the ADG uses to respond to TLSB_LOCKOUT. Lockout Mode 1 is the preferred lockout mechanism.</td></tr>
<tr><td>BCACHE_SIZE</td><td><3:2></td><td>R/W, 0</td><td>B-Cache Size. Specifies the size of the CPU B-cache. The value that the console writes in this field is derived from a value read from GBUS$MISCR. The values are assigned to cache sizes as shown below.
<table>
<tr><th><BCACHE_SIZE></th><th>Cache Size per CPU</th></tr>
<tr><td>00</td><td>Reserved</td></tr>
<tr><td>01</td><td>4 Mbyte cache per CPU</td></tr>
<tr><td>10</td><td>8 Mbyte cache per CPU</td></tr>
<tr><td>11</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>CPU1_DIS</td><td><1></td><td>R/W, 0</td><td>CPU1 Disable. When set, causes the ADG to ignore service requests from CPU1.</td></tr>
<tr><td>CPU0_DIS</td><td><0></td><td>R/W, 0</td><td>CPU0 Disable. When set, causes the ADG to ignore service requests from CPU0.</td></tr>
</table>

TLEPAERR— ADG Error Register

Address BB + 1500
Access R/W

The ADG Error Register contains CPU module error bits. These bits are set as a result of errors detected in the ADG.

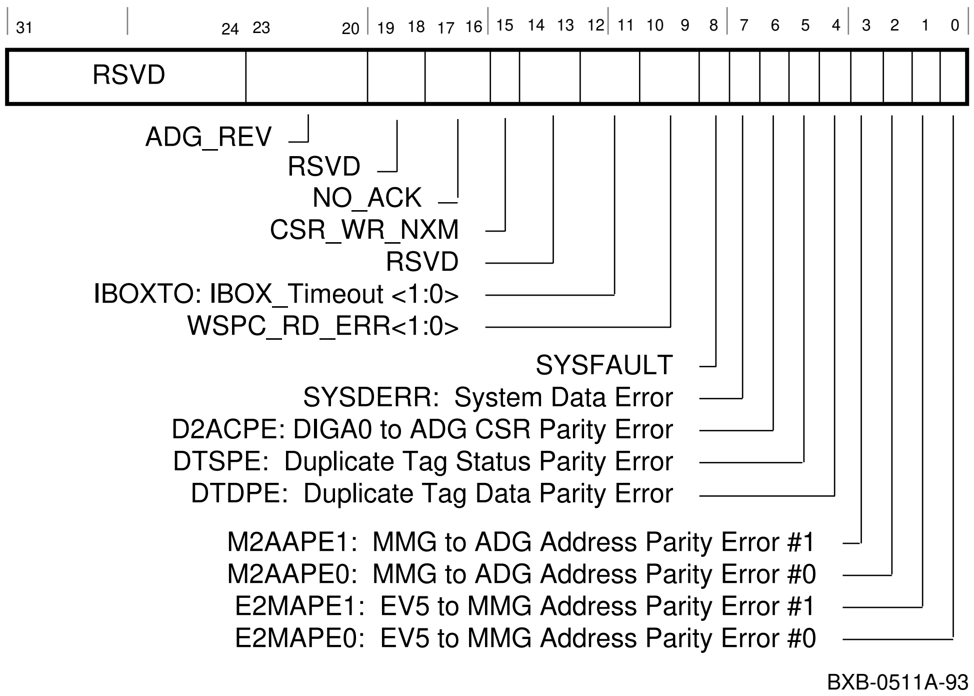

Table 2-2 TLEPAERR Register Bit Definitions

Name	Bit(s)	Type	Function
RSVD	<31:24>	R/W, 0	**Reserved.** Must be written as zeros.
ADG_REV	<23:20>	R, 6	**ADG Chip Revision.** Shows the ADG chip revision. The minimum revision number on the KN7CE is 6 (hex).
RSVD	<19:18>	R/W,	**Reserved.** Must be written as zeros.
NO_ACK	<17:16>	W1C, 0	**No Acknowledgment.** No acknowledgment from one of the DECchip 21164 processors. Bit <16> applies to CPU0; bit <17> to CPU1.
CSR_WR_NXM	<15>	R, 0	**CSR Write Not Transmitted.** CSR write to other than the TLMBPR register was not acknowledged.
RSVD	<14:13>	R, 0	**Reserved.** Read as zeros.
IBOXTO	<12:11>	W1C, 0	**Ibox Timeout.** When set, indicates that the DECchip 21164 Ibox timers have fired. Bit <11> applies to CPU0; bit <12> to CPU1.
WSPC_RD_ERR	<10:9>	W1C, 0	**Window Space Read Error.** When set, indicates a window space read error. Bit <9> applies to CPU0; bit <10> to CPU1.
SYSFAULT	<8>	W1C, 0	**System Fault.** When set, indicates that TLSB_FAULT is asserted, but not by this module.
SYSDERR	<7>	W1C, 0	**System Data Error.** Set as a result of the assertion of TLSB_DATA_ERROR. If <SYSDERR> is set and no TLBER bits are set, then <SYSDERR> is indicative of a TLSB data error detected on a module other than TLEP, but not detected on TLEP.
D2ACPE	<6>	W1C, 0	**DIGA0 to ADG CSR Parity Error.** Set when the ADG detects a parity error on CSR data transmitted from DIGA0 to the ADG. This error can occur when a CSR in the ADG is being written. This error indicates that CSR data has been corrupted. This is a hard error.
DTSPE	<5>	W1C, 0	**DTag Status Parity Error.** Set when the ADG detects a parity error on duplicate tag store status data. This error can be detected as a result of any duplicate tag read, including DTag lookups and diagnostic DTag reads. This error indicates corrupted system coherency. This is a hard error and causes a machine check.
DTDPE	<4>	W1C, 0	**DTag Data Parity Error.** Set when the ADG detects a parity error on duplicate tag store tag data. This error can be detected as a result of any duplicate tag read, including DTag lookups and diagnostic DTag reads. This error indicates corrupted system coherency. This is a hard error and causes a machine check.

Table 2-2 TLEPAERR Register Bit Definitions (Continued)

Name	Bit(s)	Type	Function
M2AAPE1	<3>	W1C, 0	**MMG to ADG Address Parity Error #1.** Set when the ADG detects a parity error on the address bus between CPU1 MMG and the ADG. A parity check is performed after the ADG has assembled the CPU address and cmd/addr parity, as piped from the MMG, and combined it with the CPU command sent directly from the CPU. This error can occur at any time when CPU1 is driving CPU1 ADDR<39:4>, CMD<3:0>, and ADDR_CMD_PAR. This is a hard error.
M2AAPE0	<2>	W1C, 0	**MMG to ADG Address Parity Error #0.** Set when the ADG detects a parity error on the address bus between CPU0 MMG and the ADG. A parity check is performed after the ADG has assembled the CPU address and cmd/addr parity, as piped from the MMG, and combined it with the CPU command sent directly from the CPU. This error can occur at any time when CPU0 is driving CPU0 ADDR<39:4>, CMD<3:0>, and ADDR_CMD_PAR. This is a hard error.
E2MAPE1	<1>	W1C, 0	**CPU to MMG Address Parity Error #1.** Set when the ADG detects a parity error on the address bus between CPU1 and the MMG. The parity check for this error is done in the MMG. The results are piped to the ADG. This error can only occur when CPU1 is driving CPU1 ADDR<39:4>, CMD<3:0>, and ADDR_CMD_PAR. This is a hard error.
E2MAPE0	<0>	W1C, 0	**CPU to MMG Address Parity Error #0.** Set when the ADG detects a parity error on the address bus between CPU0 and the MMG. The parity check for this error is done in the MMG. The results are piped to the ADG. This error can only occur when CPU0 is driving CPU0 ADDR<39:4>, CMD<3:0>, and ADDR_CMD_PAR. This is a hard error.

TLEP_VMG—Voltage Margining Register

Address BB + 15C0
Access R/W

The TLEP_VMG register is implemented in DIGA1. It drives the voltage margining circuit on the CPU module to vary the 5 V and 3.3 V supplies. The otherwise unused (on DIGA1) interrupt lines are used for this function. Any value written into this register is cleared on reset.

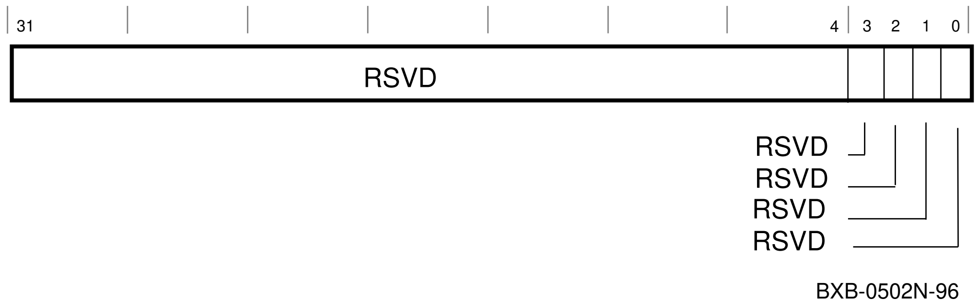

Table 2-3 TLEP_VMG Register Bit Definitions

Name	Bit(s)	Type	Function
RSVD	<31:0>	R/W, 0	**Reserved.** Must be written as zeros.

TL56WERR—Window Space Error Register (Write)

Address BB + 1600
Access W

The TL56WERR register is comprised of four read-only registers that reside at the same address. The register to be read is selected when the TL56WERR is accessed first with a write, specifying one of the four registers to be read. Subsequent to the write, a memory barrier is performed, followed by a read of the TL56WERR. The four TL56WERR registers are provided to help in the diagnosis of Ibox timeout errors. The write-only TL56WERR register is described first below. The four read-only TL56WERR registers are described next.

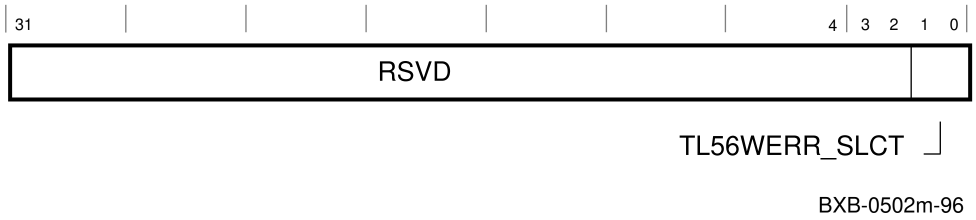

Table 2-4 TL56WERR (Write-Only) Register Bit Definitions

Name	Bit(s)	Type	Function
RSVD	<31:2>	W, 0	**Reserved.** Must be written as zeros.
TL56WERR_SLCT	<1:0>	W, U	**TL56WERR Select.** Specifies the TL56WERR register to be read in the subsequent operation as follows:

<TL56WERR_SLCT>	TL56WERR Read Register
00	0
01	1
10	2
11	3

TL56WERR—Window Space Error Register 0 (Read)

Address BB + 1600
Access R

The TL56WERR (read-only) register 0 is one of the four registers selected by first writing a zero to the same register with the value of 00 in the TL56WERR_SLCT field. This register holds address bits <19:3> of the last window space read issued by CPU0. See also TL56WERR register (write).

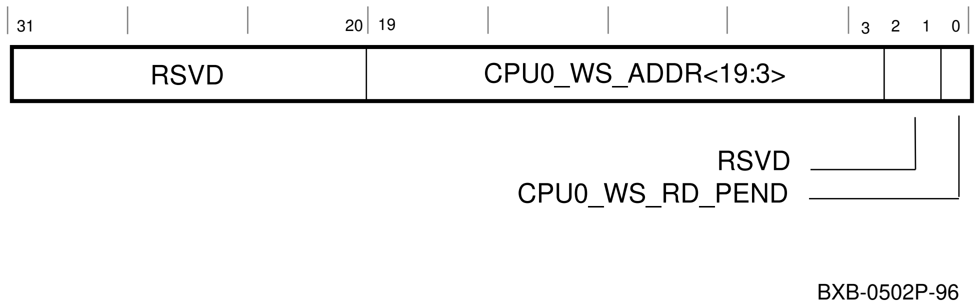

Table 2-5 TL56WERR (Read-Only) Register 0 Bit Definitions

Name	Bit(s)	Type	Function
RSVD	<31:20>	R, 0	**Reserved.** Read as zeros.
CPU0_WS_ADDR<19:3>	<19:3>	R, U	**CPU0 Window Space Address <19:3>.** Address bits <19:3> of the last window space read issued by the KN7CE CPU0.
RSVD	<2:1>	R, 0	**Reserved.** Read as zeros.
CPU0_WS_RD_PEND	<0>	R, 0	**CPU0 Window Space Read Pending.** When set, indicates that a window space read from KN7CE CPU0 is in progress.

TL56WERR—Window Space Error Register 1 (Read)

Address BB + 1600
Access R

The TL56WERR (read-only) register 1 is one of the four registers selected by first writing a zero to the same register with the value of 01 in the TL56WERR_SLCT field. This register holds address bits <38:20> of the last window space read issued by CPU0. See also TL56WERR register (write).

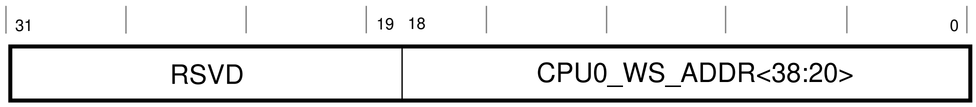

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Table 2-6 TL56WERR (Read-Only) Register 1 Bit Definitions

Name	Bit(s)	Type	Function
RSVD	<31:19>	R, 0	**Reserved.** Read as zeros.
CPU0_WS_ADDR<38:20>	<18:0>	R, U	**CPU0 Window Space Address <38:20>.** Address bits <38:20> of the last window space read issued by KN7CE CPU0.

TL56WERR—Window Space Error Register 2 (Read)

Address BB + 1600
Access R

The TL56WERR (read only) 2 register is one of the four registers selected by first writing a zero to the same register with the value of 10 in the TL56WERR_SLCT field. This register holds address bits <19:3> of the last window space read issued by CPU1. See also TL56WERR register (write).

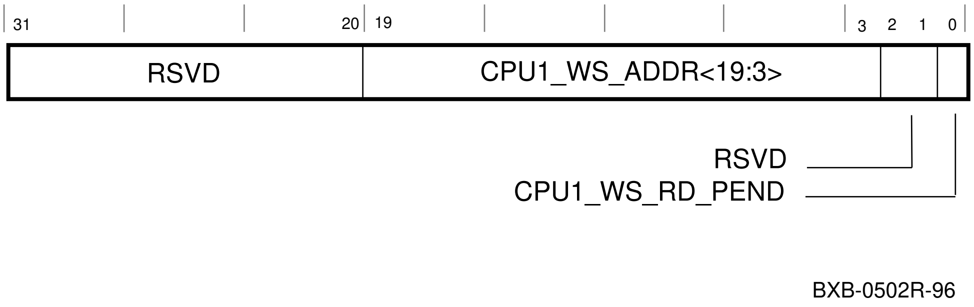

Table 2-7 TL56WERR (Read-Only) Register 2 Bit Definitions

Name	Bit(s)	Type	Function
RSVD	<31:20>	R, 0	**Reserved.** Read as zeros.
CPU1_WS_ADDR<19:3>	<19:3>	R, U	**CPU1 Window Space Address <19:3>.** Address bits <19:3> of the last window space read issued by KN7CE CPU1.
RSVD	<2:1>	R, 0	**Reserved.** Read as zeros.
CPU1_WS_RD_PEND	<0>	R, 0	**CPU1 Window Space Read Pending.** When set, indicates that a window space read from KN7CE CPU1 is in progress.

TL56WERR—Window Space Error Register 3 (Read)

Address BB + 1600
Access R

The TL56WERR (read-only) register is one of the four registers selected by first writing a zero to the same register with the value of 11 in the TL56WERR_SLCT field. This register holds address bits <38:20> of the last window space read issued by CPU1. See also TL56WERR register (write).

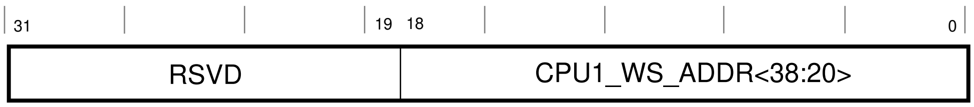

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Table 2-8 TL56WERR (Read-Only) Register 3 Bit Definitions

Name	Bit(s)	Type	Function
RSVD	<31:19>	R, 0	**Reserved.** Read as zeros.
CPU1_WS_ADDR<38:20>	<18:0>	R, U	**CPU1 Window Space Address <38:20>.** Address bits <38:20> of the last window space read issued by KN7CE CPU1.

GBUS$MISCR Register

Address FF C400 0000
Access R

The GBUS$MISCR register is used to gather various read bits that show module configuration.

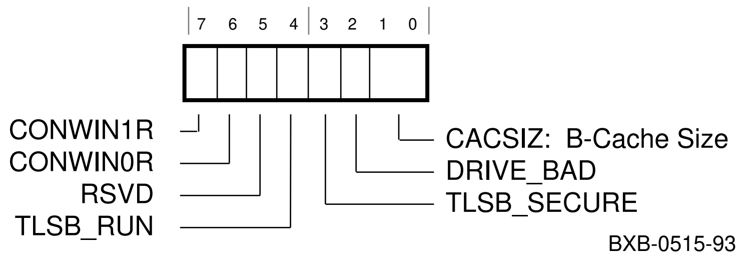

Table 2-9 GBUS$MISCR Register Bit Definitions

Name	Bit(s)	Type	Function
CONWIN1R	<7>	R, 0	**Console Winner CPU1 Read.** When set, indicates that CPU1 is running console. This is a read copy of the write-only bit implemented in GBUS$MISCW.
CONWIN0R	<6>	R, 0	**Console Winner CPU0 Read.** When set, indicates that CPU0 is running console. This is a read copy of the write-only bit implemented in GBUS$MISCW.
RSVD	<5>	R0	**Reserved.** Reads as zero.
TLSB_RUN	<4>	R, 0	**TLSB Run.** A read copy of the TLSB run line, indicating that some module is running an operating system.
TLSB_SECURE	<3>	R, 0	**TLSB Secure.** Reflects the state of the TLSB_SECURE L signal on the centerplane. This bit is also tied to ^P DUART. When set, it inhibits ^P halts.
PROCNT	<2>	R, 0	**Processor Count.** Indicates the number of CPUs on the module. When clear, there is one CPU present on the module. This is always CPU0. When set, two processors are present.
CACSIZ	<1:0>	R, X	**B-Cache Size.** Indicates the size of the B-cache.

<CACSIZ>	B-Cache Size (Mbytes)
00	Reserved
01	4
10	8
11	Reserved

Chapter 3

MEMORY CHANNEL Overview

MEMORY CHANNEL is a hardware interconnect that permits data stored in the memory of a given computing node to be replicated in the memories of all other nodes connected to a MEMORY CHANNEL bus. A write from any node to its local copy of a replicated region results in automatic hardware-based updates to the copies of all other nodes. This ability provides a memory region having properties similar to a high-performance shared memory across a group of nodes. The consistency rules between nodes using MEMORY CHANNEL are looser than traditional SMP systems, but still are very useful.

MEMORY CHANNEL significantly improves the performance of distributed systems by improving system-to-system communication latencies and bandwidths. This improvement helps bring system-to-system communication capability back in line with the individual node performance.

MEMORY CHANNEL is supported by means of a PCI Window Space based protocol.

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